DESCRIPTION

The C2467 is a high frequency step-down switching regulator with integrated internal high-side, high voltage power MOSFET. It provides 2.5A output with current mode control for fast loop response and easy compensation.
The wide 6V to 40V input range accommodates a variety of step-down applications, including those in automotive systems. A 100μA operational quiescent current allows use in battery-powered applications.
High power conversion efficiency over a wide load range is achieved by scaling down the switching frequency at light load condition to reduce the switching and gate driving losses.
The frequency foldback prevents inductor current runaway during startup and thermal shutdown provides reliable, fault tolerant operation.
The C2467 is available in thermally enhanced SOIC8 package.

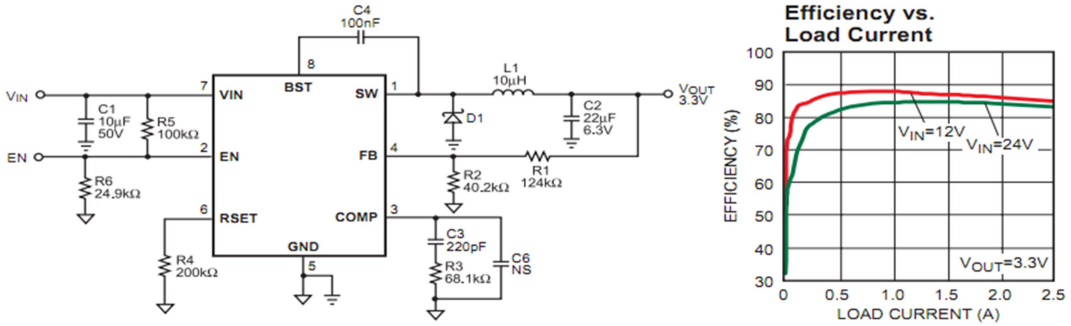
FEATURES

- 100μA Quiescent Current
- Wide 6V to 40V Operating Input Range
- 150mΩ Internal Power MOSFET
- 500kHz Fixed Switching Frequency
- Ceramic Capacitor Stable
- Internal Soft-Start
- Precision Current Limit without a Current Sensing Resistor
- Up to 95% Efficiency
- Output Adjustable from 0.8V to 30V
- Available in SOIC8 with Exposed Pad Packages

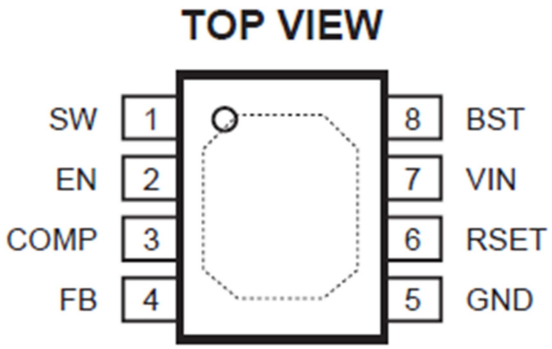
APPLICATIONS

- Game Machines
- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Printer Systems
- Battery Powered Systems

TYPICAL APPLICATION



PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN})..... ....–0.3V to 43V
Switch Voltage (V_{SW})..... ....–0.3V to V_{IN} + 0.3V
BST to SW ....–0.3V to +5V
All Other Pins..... ....–0.3V to +5V
Continuous Power Dissipation (T_A = + 25°C).....2.5W
Junction Temperature..... ....150°C
Lead Temperature ....260°C
Storage Temperature..... ....–65°C to +150°C

Recommended Operating Conditions

Supply Voltage V_{IN} ....6V to 40V
Output Voltage V_{OUT}..... ....0.8V to 30V
Operating Junct. Temp (T_J)..... .... –40°C to +125°C

Thermal Resistance θJA θJC

SOIC8E ..... 50..... 10... °C/W

ELECTRICAL CHARACTERISTICS

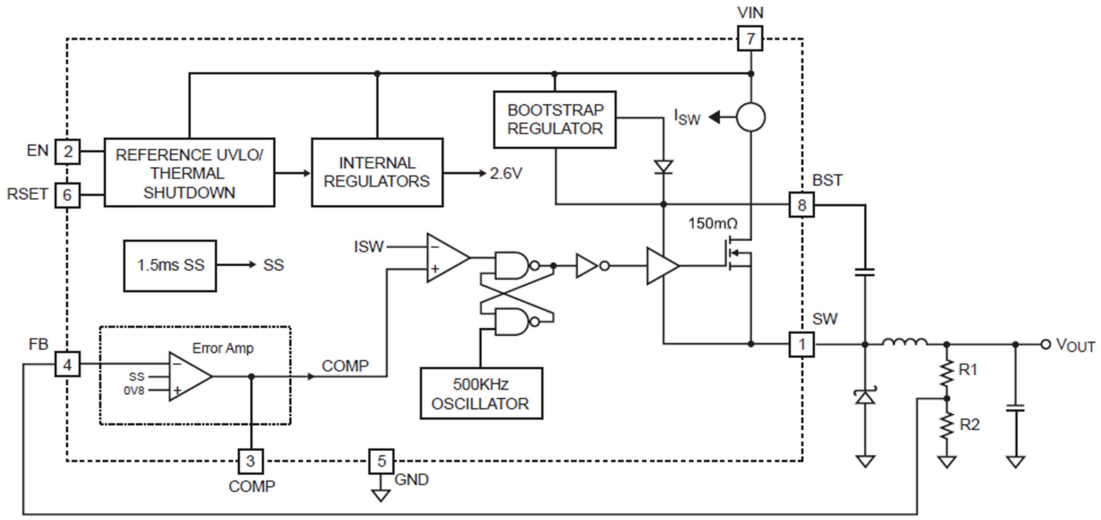
V_{IN} = 12V, V_{EN} = 2.5V, V_{COMP} = 1.4V, T_A= +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	6V < V_{IN} < 40V	0.776	0.8	0.824	V
Upper Switch On Resistance	$R_{DS(ON)}$	V_{BST} – V_{SW} = 5V		150		mΩ
Upper Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		1		μA
Current Limit			2.9	3.5		A
COMP To Current Sense Transconductance	Gcs			6		A/V
Error Amp Voltage Gain (5)				200		V/V
Error Amp Transconductance		I_{COMP} = ±3μA	40	60	80	μA/V
Error Amp Min Source current		V_{FB} = 0.7V		5		μA
Error Amp Min Sink current		V_{FB} = 0.9V		–5		μA
VIN UVLO Threshold			2.7	3.0	3.3	V
VIN UVLO Hysteresis				0.35		V
Soft-Start Time (5)		0V < V_{FB} < 0.8V		1.5		ms
Oscillator Frequency			400	500	600	KHz
Minimum Switch On Time (5)				100		ns
Shutdown Supply Current		V_{EN} = 0V		12	20	μA
Quiescent Supply Current		No load, V_{FB} = 0.9V		100	125	μA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				15		°C
EN Up Threshold			1.35	1.5	1.65	V
EN Down Threshold			1.15	1.2	1.25	V
Minimum Off Time (5)				200		ns

PIN FUNCTIONS

Pin #	Name	Description
1	SW	Switch Node. This is the output from the high-side switch. A low V_f Schottky rectifier to ground is required. The rectifier must be close to the SW pins to reduce switching spikes.
2	EN	Enable Input. Pulling this pin below the specified threshold shuts the chip down. Pulling it above the specified threshold or leaving it floating enables the chip.
3	COMP	Compensation. This node is the output of the error amplifier. Control loop frequency compensation is applied to this pin.
4	FB	Feedback. This is the input to the error amplifier. An external resistive divider connected between the output and GND is compared to the internal +0.8V reference to set the regulation voltage.
5	GND	Ground. It should be connected as close as possible to the output capacitor avoiding the high current switch paths.
6	RSET	Internal Bias Setting. Connect a 200kΩ resistor to this pin.
7	VIN	Input Supply. This supplies power to all the internal control circuitry, including bootstrap regulator and the high-side switch. A decoupling capacitor to ground must be placed close to this pin to minimize switching spikes.
8	BST	Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.

BLOCK DIAGRAM



OPERATION

The C2467 is a fixed frequency,non-synchronous, step-down switching regulator with an integrated high-side high voltage power MOSFET. It provides a single highly efficient solution with current mode control for fast loop response and easy compensation. It features a wide input voltage range, internal soft-start control and precision current limiting. Its very low operational quiescent current makes it suitable for battery powered applications.
The C2467 operates in a fixed frequency, peak current control mode to regulate the outputvoltage. A PWM cycle is initiated by the internal clock. The power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off for at least 200ns before the next cycle starts. If, in one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET remains on, saving a turn-off operation.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the external compensation network to form the COMP voltage, which is used to control the power MOSFET current.
During operation, the minimum COMP voltage is clamped to 0.9V and its maximum is clamped to 2.0V. COMP is internally pulled down to GND in shutdown mode. COMP should not be pulled above 2.6V.

Internal Regulator

Most of the internal circuitries are powered from the 2.6V internal regulator.

This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 3.0V, the output of the regulator is in full regulation. When VIN is lower than 3.0V, the output decreases.

Enable Control

The C2467 has a dedicated enable control pin(EN). With high enough input voltage, the chip can be enabled and disabled by EN. Its falling threshold is 1.2V, and its rising threshold is 1.5V (300mV higher).
If left open, EN is pulled up to about 3.0V by an internal 1μA current source. To disable the part, EN pin must be pulled down with greater than 2μA current.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The UVLO rising threshold is about 3.0V while its falling threshold is a consistent 2.6V.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 2.6V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, it shuts down the whole chip. When the temperature is lower than its lower threshold, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV.
At higher duty cycle operation condition, the time period available to the bootstrap charging may be too short to sufficiently recharge the bootstrap capacitor.
In case the internal circuit does not have sufficient voltage and the bootstrap capacitor is not charged, extra external circuitry can be used to ensure the bootstrap voltage is in the normal operational region.
The DC quiescent current of the floating driver is about 20μA. Make sure the bleeding current at the SW node is higher than this value, such that:

$$I_O + \frac{V_O}{(R1+R2)} > 20\mu A$$

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current sense MOSFET. It is then fed to the high speed current comparator for the current mode control purpose. The current comparator takes this sensed current as one of its inputs. When the power MOSFET is turned on, the comparator is first blanked till the end of the turn-on transition to avoid noise issues. The comparator then compares the power switch current with the COMP voltage. When the sensed current is higher than the COMP voltage, the comparator output is low, turning off the power MOSFET. The cycle-by-cycle maximum current of the internal power MOSFET is internally limited.

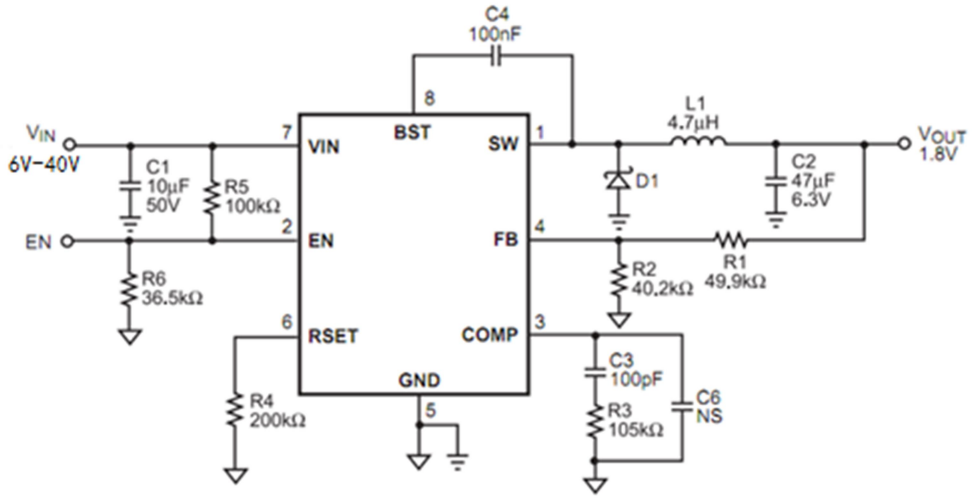
Startup and Shutdown

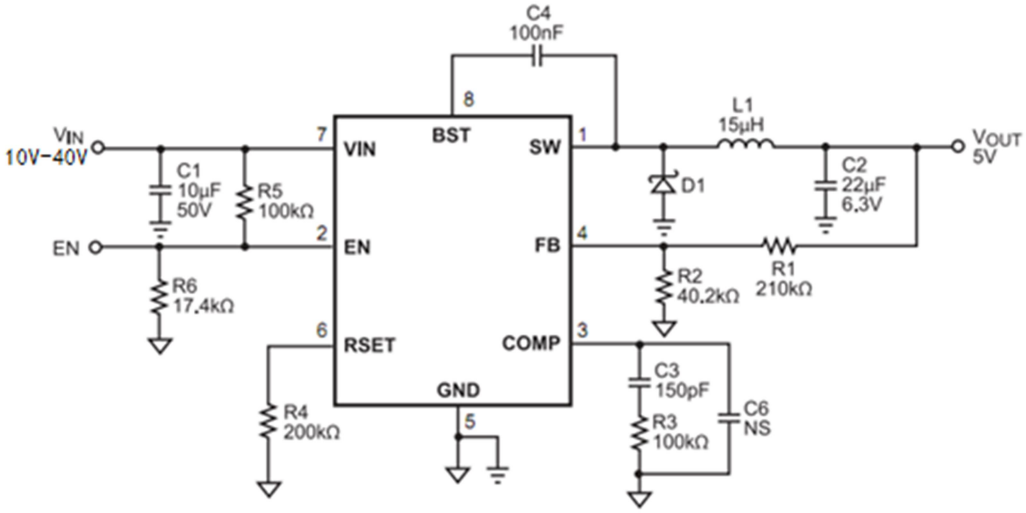
If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the signaling path of the power MOSFET turn-on at OFF for about 50μs to blank the startup glitches. When the internal soft-start block is enabled, it first holds its SS output low to ensure the reamining circuitries are ready and then slowly ramps up.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

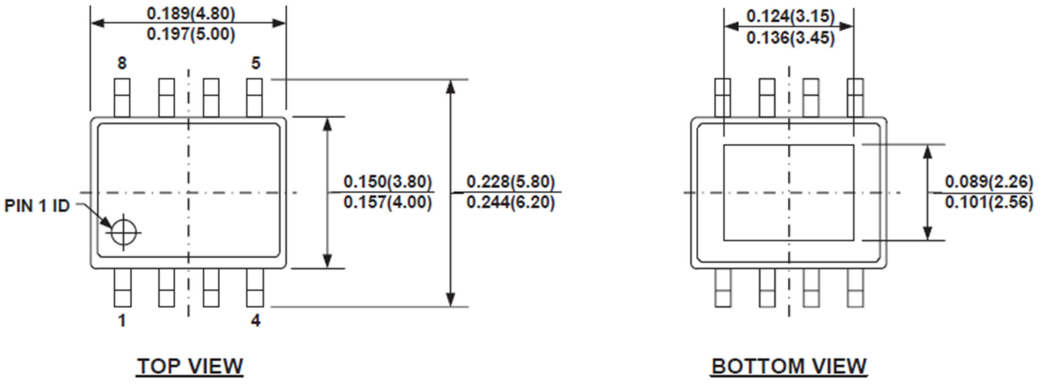
TYPICAL APPLICATION CIRCUITS

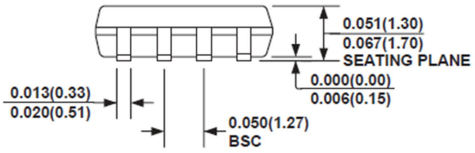




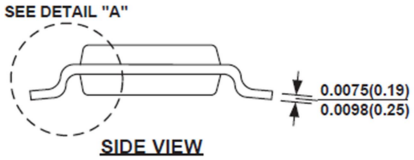
PACKAGE INFORMATION

SOIC8E (EXPOSED PAD)

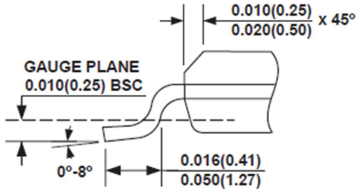




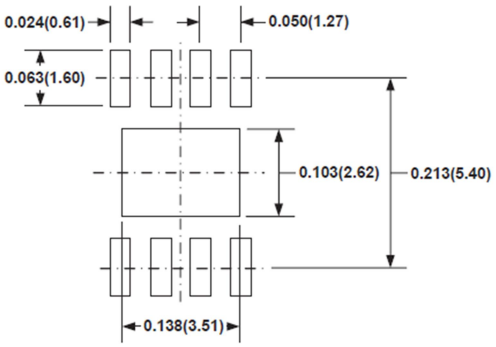
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.